REMARKS

The Official Action mailed December 19, 2002, has been received and reviewed. Claims 1, 3 through 6, 9, 10, 19, 21 through 24, 27, and 28 are currently pending in the application. All claims stand rejected. Applicant has amended claims 3 and 21 and added claims 29 through 32. Reconsideration of the application as amended herein is respectfully requested.

35 U.S.C. § 103(a) Obviousness Rejections

A) Applicable Authority

The basic requirements of a *prima facie* case of obviousness are summarized in MPEP §2143 through §2143.03. In order "[t]o establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine the reference teachings. Second, there must be a reasonable expectation of success [in combining the references]. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the expectation of success must both be found in the prior art, not in applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)." MPEP §2143. Further, in establishing a *prima facie* case of obviousness, the initial burden is placed on the Examiner. "To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed invention or the examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references." *Ex parte Clapp*, 227 USPQ 972, 973 (Bd. Pat. App. & Inter. 1985). *See also* MPEP §706.02(j) and §2142.

(B) Obviousness Rejection Based on U.S. Patent 6,124,189 to Watanabe et al. in View of U.S. Patent 6,084,304 to Huang et al.

It is stated in ¶ 2 of the outstanding *Official Action* that claims 1, 3 through 6, 9, 10, 19, 21 through 24, 27 and 28 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over

U.S. Patent 6,124,189 to Watanabe et al. (hereinafter the "Watanabe reference") in view of U.S. Patent 6,084,304 to Huang et al. (hereinafter the "Huang reference"). Applicant respectfully submits, however, that the above-stated rejection appears from the outstanding *Official Action* to actually be based upon the Watanabe reference in view of U.S. Patent 5,955,781 to Joshi et al. (hereinafter the "Joshi reference") rather than in view of the Huang reference. The text of the rejection is void of any reference to the Huang reference while the Joshi reference is specifically referred to throughout. Accordingly, the following remarks address a 35 U.S.C. § 103(a) rejection of the pending claims based upon the Watanabe reference in view of the Joshi reference. If this understanding is in error, clarification of the rejection is respectfully requested.

As the Examiner has failed to establish a *prima facie* case of obviousness based upon the Watanabe reference in view of the Joshi reference, Applicant respectfully traverses this rejection, as hereinafter set forth.

For the sake of convenience, the independent claims to which the 35 U.S.C. § 103(a) rejection applies are summarized herein. Independent claim 1 recites a contact for a semiconductor device. The contact comprises a single contact plug extending through a first barrier layer planarized down to a transistor gate member, the single contact plug in electrical communication with an active region on a semiconductor substrate. The contact further comprises an individual contact land disposed atop the single contact plug and a portion of the first barrier layer, wherein the contact land is wider than the single contact plug and *is substantially planar*. Further, the contact comprises an upper contact extending through a second barrier layer, the second barrier layer disposed over the first barrier layer, to form an electrical contact with the individual contact land.

Independent claim 3, as amended herein, recites a transistor for the dissipation of electrostatic discharges. The transistor comprises, in part, an intermediate structure comprising a substrate having at least one thick field oxide area and at least one active area including at least one implanted drain region and at least one implanted source region. The intermediate structure further includes at least one transistor gate member spanned between the at least one implanted drain region and the at least one implanted source region on the at least one active area. The transistor further comprises a first barrier layer planarized down to the at least one transistor gate

member and substantially covering the at least one thick field oxide area, the at least one active area and adjacent the at least one transistor gate member. Still further, the transistor of independent claim 3 comprises at least one drain contact plug and at least one source contact plug, both extending through the first barrier layer, an individual drain contact land disposed atop each of the at least one drain contact plugs and a portion of the first barrier layer and an individual source contact land disposed atop each of the at least one source contact plugs and a portion of the first barrier layer. The individual drain contact land is wider than the at least one drain contact plug, the individual source contact land is wider than the at least one source contact plug and *both the individual contact land and the individual source contact land are substantially planar*. A second barrier layer is disposed over the first barrier layer, the individual drain contact land and the individual source contact land. At least one upper source contact extends through the second barrier layer, the at least one upper source contact being in electrical communication with at least one of the individual source contact lands and at least one upper drain contact extends through the second barrier layer, the at least one upper drain contact being in electrical communication with at least one of the individual drain contact lands.

Independent claim 19 recites a semiconductor device including at least one contact. The semiconductor device of claim 19 comprises a single contact plug extending through a first barrier layer planarized down to a transistor gate member, the single contact plug being in electrical communication with an active region on a semiconductor substrate. The contact further comprises an individual contact land disposed atop the single contact plug and a portion of the first barrier layer, the individual contact land being wider than the single contact plug *and substantially planar*. Further, the semiconductor device comprises an upper contact extending through a second barrier layer, the second barrier layer disposed over the first barrier layer, to form an electrical contact with the individual contact land.

Independent claim 21, as amended herein, recites a semiconductor device including at least one transistor for the dissipation of electrostatic discharges. The semiconductor device comprises, in part, an intermediate structure comprising a semiconductor substrate having at least one thick field oxide area, and at least one active area including at least one implanted drain region, and at least one implanted source region. The intermediate structure further includes at

least one transistor gate member spanned between the at least one implanted drain region and the at least one implanted source region on the at least one active area. The semiconductor device further comprises a first barrier layer planarized down to the at least one transistor gate member and substantially covering the at least one thick field oxide area, the at least one active area, and adjacent the at least one transistor gate member. The transistor further comprises at least one drain contact plug and at least one source contact plug, both extending through the first barrier layer, an individual contact land disposed atop each of the at least one drain contact plugs and a portion of the first barrier layer and an individual source contact land disposed atop each of the at least one source contact plugs and a portion of the first barrier layer. The individual drain contact land is wider than the at least one drain contact plug *and substantially planar*, and the individual source contact land is wider than the at least one source contact plug *and substantially planar*. A second barrier layer is disposed over the first barrier layer. At least one upper source contact extends through the second barrier layer, the at least one upper source contact being in electrical communication with at least one of the individual source contact lands. At least one upper drain contact extends through the second barrier layer, the at least one upper drain contact in electrical communication with at least one of the individual drain contact lands.

It is respectfully submitted that a *prima facie* case of obviousness cannot be made with regard to independent claims 1, 3 (as amended herein), 19 and 21 (as amended herein) based upon the asserted combination of references as these references, whether taken alone or in combination, fail to teach or suggest each and every element of these claims.

The Watanabe reference discloses a metal strapped polysilicon gate metallization structure for a semiconductor device and method of forming the same. *See*, *Watanabe reference*, Abstract, col. 2, lines 18-20. The metal strapped polysilicon gate structure of the Watanabe reference includes a p-type silicon substrate 100 having an active area which is isolated from other elements by shallow trench isolation regions 101. Spaced apart source/drain diffusion regions 107 are formed in the substrate and a gate structure 130 is insulatively spaced from a channel region between the source/drain regions 107 by a gate dielectric film 102. *See id.*, col. 3, lines 37-55. An insulating layer 108 is formed on the silicon substrate 100, the shallow trench isolation regions 101 and the source/drain regions 107. *See id.*, FIG. 7B, col. 5, line 65–col. 6,

line 10. Contact openings 109 are formed in the insulating layer 108 and include a titanium/titanium nitride layer 110 on the sidewalls thereof. *See id.*, col. 6, lines 9-12. The contact openings 109 are filled with a conductive material layer 111C. A second insulating layer 112 is formed over the first insulating layer 108 and openings 113 are formed therein. The openings are filled with a conductive material to form wiring layer 114. *See id.*, FIG. 7B, col. 6, lines 15-20.

Applicant submits that the wiring layer 114 of the Watanabe reference is not a contact land as claimed in each of independent claims 1, 3, 19 and 21. Instead, the wiring layer 114 is similar to the source contact metallization 252 and drain contact metallization 254 as described in the present application with reference to the prior art. *See*, *Specification*, ¶ **[0007]**, FIG. 38. Even if the wiring layer 114 may be used to form multilevel structures, as asserted in the outstanding *Official Action*, it is not a contact land for helping reduce problems associated with etch misalignments.

Further, it is stated in the outstanding *Official Action* that the Watanabe reference discloses "[a]n individual contact land (114) disposed atop said single contact plug and a portion of said first barrier layer, wherein said contact land is wider than said single contact plug and *is substantially planar*" (emphasis added). *Official Action*, ¶ 4. Applicant respectfully submits, however, that the wiring layer 114 of the Watanabe reference is ***not*** substantially planar as asserted and recited in each of independent claims 1, 3, 19 and 21 of the referenced application. It is readily apparent from FIG. 7B of the Watanabe reference that the wiring layer 114 is not substantially planar but rather has a stepped configuration transitioning between the second insulating layer 112 and the first insulating layer 108. *See*, *Watanabe reference*, FIG. 7B.

It is respectfully submitted that the limitations of claims 1, 3 (as amended), 19 and 21 (as amended) are also not disclosed by the Joshi reference. In fact, the Joshi reference fails to disclose a contact land at all, let alone one which is substantially planar. Accordingly, it is respectfully submitted that the combination of the Watanabe and the Joshi reference fails to teach or suggest each of the limitations of independent claims 1, 3 (as amended), 19 and 21 (as amended) of the referenced application.

It is further respectfully submitted that a *prima facie* case of obviousness cannot be established based upon the asserted combination of references as there is no suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine the reference teachings. As stated above, the Watanabe reference discloses a polysilicon gate metallization structure for a semiconductor device and method of forming the same. The Joshi reference, on the other hand, discloses thermal conductors embedded within a semiconductor for dissipating heat from the semiconductor structure and methods of forming such thermal conductors. There is no suggestion or motivation, either from the references or in the knowledge generally available to one of ordinary skill in the art, which would lead one to examine the thermal conductors of the Joshi reference in order to modify the methods of forming a polysilicon gate metallization structure as disclosed in the Watanabe reference. "Before the PTO may combine the disclosures of two or more prior art references in order to establish *prima facie* obviousness, **there must be some suggestion for doing so** . . ." *In re Fine*, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598-99 (Fed. Cir. 1988) (emphasis added). "The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." *In re Gordon*, 733 F.2d at 902, 221 USPQ at 1127 (Fed. Cir. 1984). Absent such a suggestion to make the asserted modification, it is respectfully submitted that the Examiner has used impermissible "hindsight" occasioned by the Applicant's teachings to hunt through the prior art for the claimed elements and combine them as claimed. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). It is respectfully submitted that such is not an appropriate basis for determining patentability."

In view of the foregoing, Applicant respectfully submits that the cited references fail to establish a *prima facie* case of obviousness of independent claims 1, 3, 19 and 21. Accordingly, it is respectfully requested that the rejections under 35 U.S.C. § 103(a) of claims 1, 3, 19 and 21 based upon the asserted combination of the Watanabe and Joshi references be withdrawn. Claims 1, 3, 19 and 21 are believed to be in condition for allowance and such favorable action is respectfully requested.

Each of the dependent claims of the present application is also believed to be in condition for allowance because the independent claims from which they depend are in condition for allowance. *See*, *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988)(dependent claims are nonobvious under 35 U.S.C. § 103(a) if the independent claims from which they depend are nonobvious). Thus, it is respectfully requested that the obviousness rejections of claims 4 through 6, 9, 10, 22 through 24, 27 and 28 be withdrawn as well.

Each of claims 1, 3 through 6, 9, 10, 19, 21 through 24, 27 and 28 is believed to be in condition for allowance and such favorable action is respectfully requested.

NEW CLAIMS

Claims 29 through 32 have been added by way of the present communication. New independent claim 29 recites a contact for a semiconductor device. The contact comprises a single contact plug extending through a first barrier layer and a second barrier layer. The second barrier layer is disposed over the first barrier layer and planarized down to a transistor gate member and the single contact plug is in electrical communication with an active region on a semiconductor substrate. The contact further comprises an individual contact land disposed atop the single contact plug and a portion of the second barrier layer, the individual contact land being wider than the single contact plug. Still further, the contact comprises an upper contact extending through a third barrier layer, the third barrier layer disposed over the second barrier layer, to form an electrical contact with the individual contact land.

New independent claim 30 recites a transistor for the dissipation of electrostatic discharges. The transistor comprises an intermediate structure comprising a substrate having at least one thick field oxide area and at least one active area. The at least one active area includes at least one implanted drain region and at least one implanted source region. The intermediate structure further includes at least one transistor gate member spanned between the at least one implanted drain region and the at least one implanted source region on the at least one active area. The transistor further comprises a first barrier layer substantially covering the at least one thick field oxide area and the at least one active area, and adjacent the at least one transistor gate member. Still further, the transistor comprises a second barrier layer disposed over said first barrier layer and planarized down to the at least one transistor gate member. At least one drain contact plug and at least one source contact plug extend through each of the first and second barrier layers, the at least one drain contact plug being in electrical communication with the at least one drain region on the semiconductor substrate and the at least one source contact plug being in electrical communication with the at least one source region on said semiconductor substrate. Further, the transistor comprises an individual drain contact land disposed atop each of the at least one drain contact plugs and a portion of the second barrier layer, the individual drain contact land being wider than the at least one drain contact plug. An individual source contact land is disposed atop each of said at least one source contact plugs and a portion of said second

barrier layer, the individual source contact land being wider than the at least one source contact plug. A third barrier layer is disposed over the second barrier layer, the individual drain contact land, and the individual source contact land. At least one upper source contact extends through the third barrier layer, the at least one upper source contact being in electrical communication with the individual source contact land. At least one upper drain contact extends through the third barrier layer, the at least one upper drain contact being in electrical communication with the individual drain contact land.

New independent claim 31 recites a semiconductor device including at least one contact. The semiconductor device comprises a single contact plug extending through each of a first barrier layer and a second barrier, the second barrier layer disposed over the first barrier layer and planarized down to a transistor gate member. The single contact plug is in electrical communication with an active region on a semiconductor substrate. The semiconductor device further includes an individual contact land disposed atop the single contact plug and a portion of the second barrier layer, the individual contact land being wider than the single contact plug. Still further, the semiconductor device comprises an upper contact extending through a third barrier layer, the third barrier layer disposed over the second barrier layer, to form and electrical contact with the individual contact land.

New independent claim 32 recites a semiconductor device including at least one transistor for the dissipation of electrostatic discharge. The semiconductor device comprises an intermediate structure comprising a semiconductor substrate having at least one thick field oxide area, and at least one active area including at least one implanted drain region, and at least one implanted source region. The intermediate structure further includes at least one transistor gate member spanned between the at least one implanted drain region and the at least one implanted source region on the at least one active area. The semiconductor device further comprises a first barrier layer substantially covering the at least one thick field oxide area, the at least one active area, and adjacent the at least one transistor gate member. Still further, the semiconductor device comprises a second barrier layer disposed over the first barrier layer and planarized down to the at least one transistor gate member, at least one drain contact plug extending through each of the first and second barrier layers and at least one source contact plug extending through each of the

first and second barrier layers. The at least one drain contact plug is in electrical communication with the at least one implanted drain region on the semiconductor substrate and the at least one source contact plug is in electrical communication with the at least one implanted source region on the semiconductor substrate. Further, the semiconductor device comprises an individual drain contact land disposed atop the at least one drain contact plug and a portion of the second barrier layer, the individual drain contact land being wider than the at least one drain contact plug, and an individual source contact land disposed atop the at least one source contact plug and a portion of the second barrier layer, the individual source contact land being wider than the at least one source contact plug. The semiconductor device further comprises a third barrier layer disposed over the second barrier layer, the individual source contact land and the individual drain contact land. At least one upper source contact extends through the third barrier layer and at least one upper drain contact extends through the third barrier layer. The at least one upper source contact is in electrical communication with the individual source contact land and the at least one upper drain contact is in electrical communication with the individual drain contact land.

It is respectfully submitted that new claims 29 through 32 are supported by the as-filed specification and that no new matter is added by way of the addition of these claims.

CONCLUSION

Claims 1, 3 through 6, 9, 10, 19, 21 through 24 and 27 through 32 are believed to be in condition for allowance and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicant's undersigned attorney.

Respectfully submitted,

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Enclosure: Version of Claims With Markings to Show Changes Made

Document in ProLaw

VERSION WITH MARKINGS TO SHOW CHANGES MADE

Claims 3 and 21 have been amended herein as follows:

3. (Six Times Amended) A transistor for the dissipation of electrostatic discharges, comprising:

an intermediate structure comprising a substrate having at least one thick field oxide area, and at least one active area including at least one implanted drain region, and at least one implanted source region, said intermediate structure further including at least one transistor gate member spanned between said at least one <u>implanted</u> drain region and said at least one <u>implanted</u> source region on said at least one active area;

a first barrier layer planarized down to said at least one transistor gate member and substantially covering said at least one <u>thick</u> field oxide area, said at least one active area, and adjacent said at least one transistor gate member;

at least one drain contact plug extending through said first barrier layer, wherein said at least one drain contact plug is in electrical communication with said at least one drain region on said semiconductor substrate;

at least one source contact plug extending through said first barrier layer, wherein said at least one source contact plug is in electrical communication with said at least one source region on said semiconductor substrate;

an individual drain contact land disposed atop each of said at least one drain contact plugs and a portion of said first barrier layer, said individual drain contact land wider than said at least one drain contact plug and substantially planar;

an individual source contact land disposed atop each of said at least one source contact plugs and a portion of said first barrier layer, said individual source contact land wider than said at least one source contact plug and substantially planar;

a second barrier layer disposed over said first barrier layer, said individual drain contact land, and said individual source contact land;

at least one upper source contact extending through said second barrier layer, said at least one upper source contact ~~is~~ in electrical communication with at least one of said individual source contact lands; and

at least one upper drain contact extending through said second barrier layer, said at least one upper drain contact in electrical communication with at least one of said individual drain contact lands.

21. (Six Times Amended) A semiconductor device including at least one transistor for the dissipation of electrostatic discharges, comprising:

an intermediate structure comprising a semiconductor substrate having at least one thick field oxide area, and at least one active area including at least one implanted drain region, and at least one implanted source region, said intermediate structure further including at least one transistor gate member spanned between said at least one implanted drain region and said at least one implanted source region on said at least one active area;

a first barrier layer planarized down to said at least one transistor gate member and substantially covering said at least one thick field oxide area, said at least one active area, and adjacent said at least one transistor gate member;

at least one drain contact plug extending through said first barrier layer, wherein said at least one drain contact plug is in electrical communication with said at least one implanted drain region on said semiconductor substrate;

at least one source contact plug extending through said first barrier layer, wherein said at least one source contact plug is in electrical communication with said at least one implanted source region on said semiconductor substrate;

an individual drain contact land disposed atop said at least one drain contact plug and a portion of said first barrier layer, said individual drain contact land wider than said at least one drain contact plug <u>and substantially planar</u>;

an individual source contact land disposed atop said at least one source contact plug and a portion of said first barrier layer, said individual source contact land ~~is~~ wider than said at least one source contact plug <u>and substantially planar</u>;

a second barrier layer disposed over said first barrier layer;

at least one upper source contact extending through said second barrier layer, said at least one upper source contact in electrical communication with at least one said individual source contact land; and

at least one upper drain contact extending through said second barrier layer, said at least one upper drain contact in electrical communication with at least one said individual drain contact land.

The following claims 29 through 32 have been added:

29. (New) A contact for a semiconductor device, comprising:

a single contact plug extending through a first barrier layer and a second barrier layer, said second barrier layer disposed over said first barrier layer and planarized down to a transistor gate member, said single contact plug being in electrical communication with an active region on a semiconductor substrate;

an individual contact land disposed atop said single contact plug and a portion of said second barrier layer, wherein said individual contact land is wider than said single contact plug;

an upper contact extending through a third barrier layer, said third barrier layer disposed over said second barrier layer, to form an electrical contact with said individual contact land.

30. (New) A transistor for the dissipation of electrostatic discharges, comprising:

an intermediate structure comprising a substrate having at least one thick field oxide area, and at least one active area including at least one implanted drain region, and at least one implanted source region, said intermediate structure further including at least one transistor gate member spanned between said at least one implanted drain region and said at least one implanted source region on said at least one active area;

a first barrier layer substantially covering said at least one thick field oxide area and said at least one active area, and adjacent said at least one transistor gate member;

a second barrier layer disposed over said first barrier layer and planarized down to said at least one transistor gate member;

at least one drain contact plug extending through each of said first and second barrier layers, wherein said at least one drain contact plug is in electrical communication with said at least one drain region on said semiconductor substrate;

at least one source contact plug extending through each of said first and second barrier layers, wherein said at least one source contact plug is in electrical communication with said at least one source region on said semiconductor substrate;

an individual drain contact land disposed atop each of said at least one drain contact plugs and a portion of said second barrier layer, said individual drain contact land wider than said at least one drain contact plug;

an individual source contact land disposed atop each of said at least one source contact plugs and a portion of said second barrier layer, said individual source contact land wider than said at least one source contact plug;

a third barrier layer disposed over said second barrier layer, said individual drain contact land, and said individual source contact land;

at least one upper source contact extending through said third barrier layer, said at least one upper source contact in electrical communication with said individual source contact land; and

at least one upper drain contact extending through said third barrier layer, said at least one upper drain contact in electrical communication with said individual drain contact land.

31. (New) A semiconductor device including at least one contact, comprising:

a single contact plug extending through each of a first barrier layer and a second barrier layer, said second barrier disposed over said first barrier layer and planarized down to a transistor gate member, said single contact plug being in electrical communication with an active region on a semiconductor substrate;

an individual contact land disposed atop said single contact plug and a portion of said second barrier layer, said individual contact land being wider than said single contact plug; and

an upper contact extending through a third barrier layer, said third barrier layer disposed over said second barrier layer, to form an electrical contact with said individual contact land.

32. (New) A semiconductor device including at least one transistor for the dissipation of electrostatic discharges, comprising:

an intermediate structure comprising a semiconductor substrate having at least one thick field oxide area, and at least one active area including at least one implanted drain region, and at least one implanted source region, said intermediate structure further including at least one transistor gate member spanned between said at least one implanted drain region and said at least one implanted source region on said at least one active area;

a first barrier layer substantially covering said at least one thick field oxide area and said at least one active area, and adjacent said at least one transistor gate member;

a second barrier layer disposed over said first barrier layer and planarized down to said at least one transistor gate member;

at least one drain contact plug extending through each of said first and second barrier layers, wherein said at least one drain contact plug is in electrical communication with said at least one implanted drain region on said semiconductor substrate;

at least one source contact plug extending through each of said first and second barrier layers, wherein said at least one source contact plug is in electrical communication with said at least one implanted source region on said semiconductor substrate;

an individual drain contact land disposed atop said at least one drain contact plug and a portion of said second barrier layer, said individual drain contact land being wider than said at least one drain contact plug;

an individual source contact land disposed atop said at least one source contact plug and a portion of said second barrier layer, said individual source contact land being wider than said at least one source contact plug;

a third barrier layer disposed over said second barrier layer, said individual source contact land and said individual drain contact land;

at least one upper source contact extending through said third barrier layer, said at least one upper source contact being in electrical communication with said individual source contact land; and

at least one upper drain contact extending through said third barrier layer, said at least one upper drain contact being in electrical communication with said individual drain contact land.